

## Transient Voltage Suppressors Array for ESD Protection

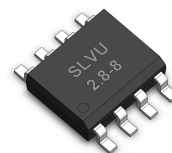
Low Capacitance

### SLVU2.8-8

#### Description

The SLVU2.8-8 is in an SO-08 package and may be used to protect two high-speed line pairs. The “flow-thru” design minimizes trace inductance and reduces voltage overshoot associated with ESD events. The low clamping voltage of the SLVU2.8-8 minimizes the stress on the protected IC.

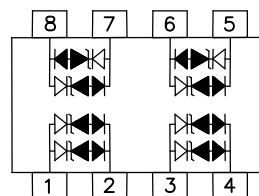
SO-08



#### Feature

- u 600 Watts Peak Pulse Power per Line (tp=8/20μs)
- u Protects eight lines (four line Pairs)
- u Low capacitance
- u RoHS Compliant
- u IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- u IEC61000-4-4 (EFT) 40A (5/50ns)
- u IEC61000-4-5 (Lightning) 24A (8/20μs)

#### Functional Diagram



#### Applications

- u WAN/LAN Equipment
- u Test & Measurement Equipment
- u Switching Systems
- u Instrumentation
- u DSLAMs
- u Base Stations
- u Analog Inputs

#### Mechanical Data

- u Molding Compound Flammability Rating : UL 94V-0
- u Weight 70 Milligrams (Approximate)
- u Quantity Per Reel : 500pcs
- u Reel Size : 7 inch
- u Lead Finish : Lead Free

#### Mechanical Characteristics

Symbol	Parameter	Value	Units
P <sub>PP</sub>	Peak Pulse Power (tp=8/20μs waveform)	600	W
T <sub>L</sub>	Lead Soldering Temperature	260 (10sec)	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to +150	°C
T <sub>J</sub>	Operating Temperature Range	-55 to +150	°C
	IEC61000-4-2 (ESD)		
	Air Discharge	±15	KV
	Contact Discharge	±8	
	IEC61000-4-4 (EFT)	40	A
	IEC61000-4-5 ( Lightning )	24	A

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### SLVU2.8-8

Electrical Characteristics (@ 25°C Unless Otherwise Specified)

Part Number	Device Marking	$V_{RWM}$ (V) (Max.)	$V_B$ (V) (Min.)	$I_T$ (mA)	$V_C$ @5A (Max.)	$V_C$		$I_R$ ( $\mu$ A) (Max.)	$C$ (pF) (Typ.)
						(Max.)	(@A)		
SLVU2.8-8	SLVU 2.8-8	2.8	3.0	1	8.5	20	24	5	5

### Characteristic Curves

Fig1. 8/20 $\mu$ s Pulse Waveform

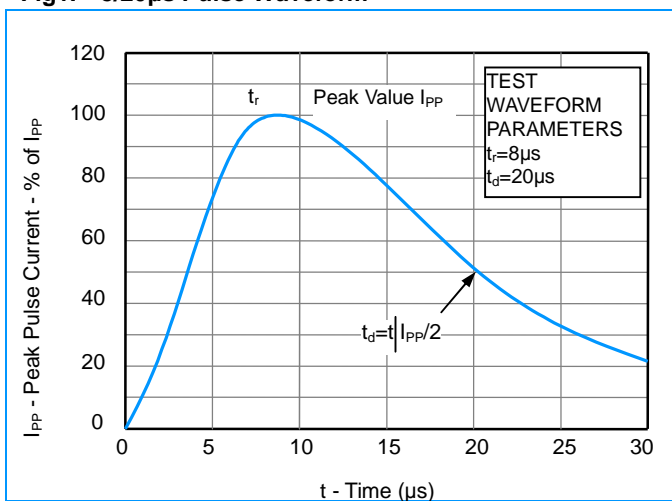


Fig2. ESD Pulse Waveform (according to IEC 61000-4-2)

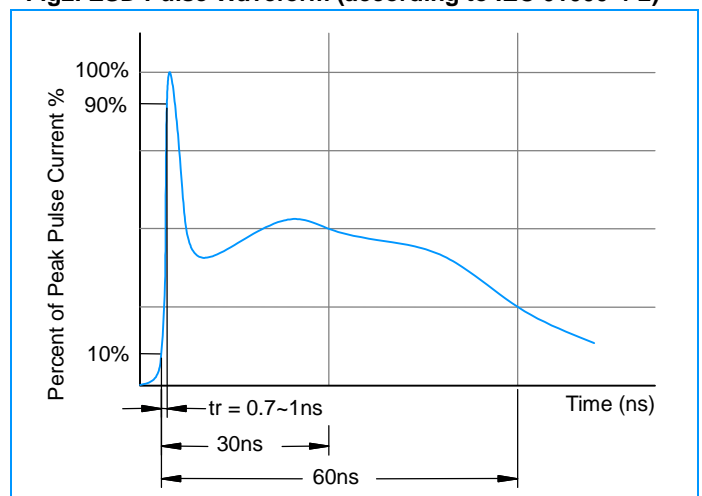


Fig3. Non - Repetitive Peak Pulse Power vs. Pulse Time

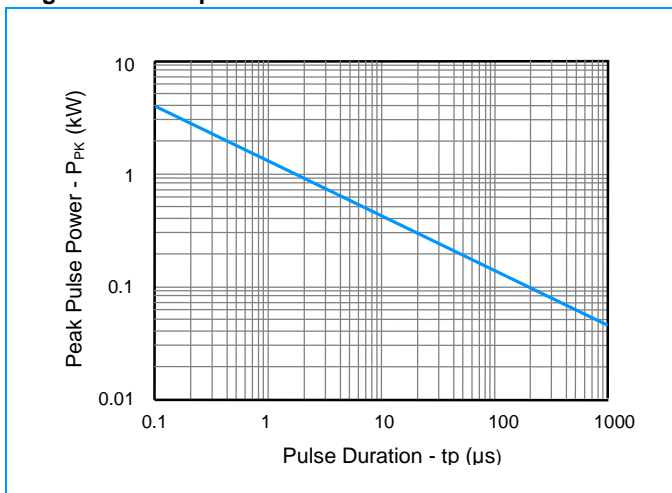
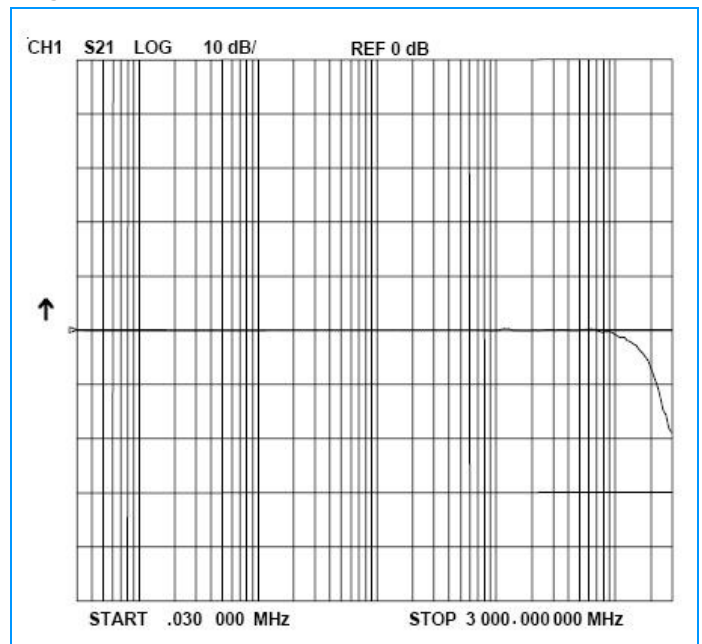


Fig4. Insertion Loss S21



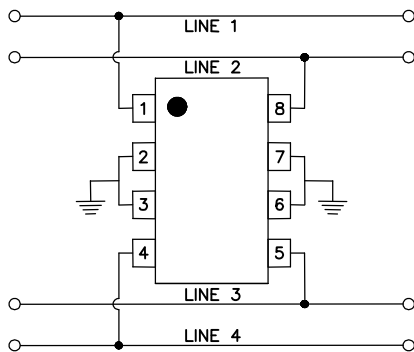


### SLVU2.8-8

#### Applications Note

Electronic equipment is susceptible to damage caused by Electrostatic Discharge (ESD), Electrical Fast Transients (EFT), and tertiary lightning effects. Knowing that equipment can be damaged, the SLVU2.8-8 was designed to provide the level of protection required to safe guard sensitive equipment. This product can be used in different configurations to provide a level of protection to meet unidirectional line requirements as well as bidirectional requirements either in a common-mode or differential-mode configuration.

**Figure 1. Unidirectional Common-Mode Protection**



#### Unidirectional Common-Mode Protection (Figure1)

The SLVU2.8-8 provides up to four lines of protection in a common-mode configuration as depicted in figure 1.

Circuit connectivity is as follows:

- Line 1 is connected to Pin 1
- Line 2 is connected to Pin 8
- Line 3 is connected to Pin 5
- Line 4 is connected to Pin 4
- Pins 2, 3, 6 and 7 are connected to ground

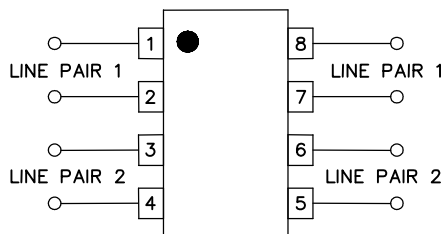
#### Bidirectional Differential-Mode Protection (Figure2)

The SLVU2.8-8 provides up to four lines of protection in a differential-mode configuration as depicted in figure 2.

Circuit connectivity is as follows:

- Line Pair 1 is connected to Pins 1 & 2
- Line Pair 2 is connected to Pins 3 & 4
- Line Pair 3 is connected to Pins 7 & 8
- Line Pair 4 is connected to Pins 5 & 6

**Figure 2. Bidirectional Differential-Mode Protection**



#### Circuit Board Layout Recommendations

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- The path length between the TVS device and the protected line should be minimized.
- All conductive loops including power and ground loops should be minimized.
- The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.